IN THE SPECIFICATION:

Page 4, last paragraph

In the illustrated embodiment, this bit stream is over- sampled by an eight times oversampler 17. Although an eight times over-sampler circuit is shown, any modulus of over-sampler, *e.g.,* 5, can be used without departing from the spirit and scope of the present invention. More generally, what occurs is that data transmitted at a first frequency is over-sampled using an effective clock at a second frequency, n times the receiver clock. In the example, n is eight but could also be some other number. This produces nominally n samples per bit time (also referred to as a unit interval), where n is an integer greater than one.

Page 5, third paragraph

As will be explained in more detail below, in the illustrative embodiment, over-sampler 17 provides n outputs, where n=8, *e.g.,* one of the groups 22a-d of eight in Fig. 2, corresponding to the eight samples. These are inputs to a sample word register 19. The sample word register 19 stores m, where, in the illustrated embodiment, m=4, successive groups of eight outputs from the oversampler 17 and outputs them as an (m x n)-bit word at a frequency 1/m that of the data frequency. In the illustrated embodiment, the word is a 32 bit word. (Actually, 40 bits are output, the additional eight bits constituting a duplicate of the oldest eight bit sample). This permits the remainder of the processing to be carried out at this lower frequency greatly reducing the demands placed on the hardware. Again m=4 is only an example and m may be of some other value, *i.e.,* m is an integer greater than 1.